

## Focus

Application-oriented design technology for micro and nano electronics has become a very important success factor for European micro and nano Electronics companies and will be looked at in its full range. Exhaustive research and development in this area has been supported by ENIAC and CATRENE and local governments through the past years. Latest results and exciting highlights from CATRENE and ENIAC projects will form the subjects of this conference.

## Contents

All CATRENE and ENIAC projects related to electronic system design, to design technology and to manufacturing topics are invited to contribute to the conference. Each project may organize a full session made of one tutorial presentation (45 min.) and 2 technical presentations (20 min. each) or contribute to a global session with a tutorial or a technical presentation.

## Steering Committee

J. Borel, R&D, France,  
B. Candaele, Thales Group, France,  
M. Coppola, ST, France,  
P. Koch, CATRENE, EU, FhG  
Manfred Dietrich, Germany  
A. Jerraya, CEA, France,  
W. John, SIL, Germany,  
Christian Sebeke, Bosch, Germany,  
Prof Dr, W. Rosenstiel, Uni. Tuebingen & FZI,  
Ralf Pferdenges, Infineon, Germany,  
K. Veelenturf, NXP, Netherlands,  
Anne Marie FOUILLIART, Thales Group, France  
Petrot TIMA, France,  
Jose Calero, DS2,  
S Eugenio Villar, Cantabria Univ, Sweden,  
Mario Diaz Nava, ST, France,  
Mart Coenen, EMC MCC, Netherlands

## Preliminary Programme

### Wednesday 23<sup>rd</sup> June

**09:00** **Welcome**

**09:15** **Opening & Keynotes**

#### Opening

*Laurent Malier, Director of Leti, CEA, France*

**09:30** **Keynote : Design in a fast moving wireless industry - The challenges of managing complexity and time to market**

*Jorgen Lantto, CTO, STE, Sweden*

**10:00** **Keynote: Technological and economical challenges of the SoC companies for the upcoming CMOS generations**

*Jean-Marc Chery, CTO ST, France*

**10:30** **Break**

### Technical Session 1 : HW and SW for Multiprocessors and many cores

*Chair : Anne-Marie Fouilliant, Thales*

**11:00** **Tutorial : TSAR Cache-Coherent Architecture**

*Prof. Alain Greiner, UPMC, France*

**11:45** **Specification and Validation of CC protocol**

*Huy-Nam Nguyen, BULL, France*

**12:05** **SoftSOC HDS Architecture**

*Marcos Martinez, ES2, Spain*

**12:30** **Lunch**

### Technical Session 2 : Smart Lighting

*Chair : Paul Merkus, Philips, Netherlands*

**14:00** **Tutorial Lighting systems based on Solid-State Lighting devices**

*Theo Treuniet, Philips, Netherlands*

**14:45** **Implementation of LED lighting in a residential show room**

*Jean-Louis Lovato, Schneider Electric, France*

**15:05** **LED : a new era for lighting**

*Patrick Mottier, LETI, France*

**16:00** **Break**

**16:30** **Panel : ID Security and Biometrics Drivers and demand for sophisticated design methods and tools for electronic components embedded software and related systems**

*Chair : Christian Sebeke, Bosch, Laurent Vibert, Gemalto, Bernard Candaele, Thales, Claudia Eckert, Fraunhofer SIT, Detlef Houdeau, Infineon, Laurent Sourgen, ST,*

### Technical Session 3 : European EDA SMEs – key for innovation

*Chair : Andreas Ripp, MunEDA,*

**18:00** *Introduction and Overview presentation by Brieuc Turluche, CEO CWS Coupling Wave Solutions and Andreas Ripp CMO & Managing Director, MunEDA*

**18:15** **Infiniscale**

*Firas Mohamed, President & CEO*

**18:30** **Edxact S.A.**

*Mathias Silvant, CEO*

**18:45** **Magillem Design Services**

*Emmanuel Vaumorin, Strategic Projects Manager*

**19:00** **Panel Session challenges for European EDA SMEs in global markets.**

*Moderator : Andreas Ripp, MunEDA,*

*Panelists :*

*Peter Feist, CEO Onespin Solution,*

*Gislain Kaiser, CEO DoceaPower,*

*Michel Tabusse, CEO Satin-IP,*

*Brieuc Turluche, CEA CWS Coupling Wave Solutions*

*Eric Beisser, CEO Xyalis*

**19:45** **End**

20:00 Social Event : dinner

**Thursday, 24<sup>th</sup> June**

**Keynotes**

09:30 **IP & Re-Use – the next wave of a successful model !**  
*Christoph Heer, VP for Digital IP and Reuse, Infineon, Germany*

10:00 **Linking Design and Fabrication technologies**  
*Michel Brillouet, Fellow, LETI, France*

10:30 **Break**

**Technical Session 4 : 3D Integration**

*Chair : Mario Diaz Nava,*

11:00 **Tutorial : Present and Future of 3D Integration**  
*Jean-Marc Yannou, YOLE, France*

11:40 **Development of CAD Tools for 3D-Integration**  
*Heiko Dudek, Cadence*

12:05 **Perspectives of Heterogenous Systems using 3D-Integration technology**  
*Peter Ramm, Fraunhofer IZM Munich, Germany*

12:30 **Lunch**

**Technical Session 5 : Low Power Design**

*Chair : Macello Coppola, ST*

14:00 **Tutorial : Power efficient designs form PA and RF to Baseband, from System level to IC implementation**  
*Bernard Candaele, Thales*

14:45 **Top down methodology for SoC power management based on a programmable controller**  
*Patrick Valdenaire, STE*

15:05 **Spidergon STNoC overview, and low power specific features**  
*Michael Soulie, ST, France*

16:00 **Break**

**Technical Session 6 : Advanced Test Technologies**

*Chair : Kees Veelenturf, NXP*

16:30 **Tutorial : Test and Dependability of Microsystems**  
*Serge Bernard, LIRMM and Philippe Cauvet, Ophimalia, France*

17:15 **Evaluation of Parametric Test Metrics for Mixed-signal/RF DFT Solutions using Statistical Techniques",**  
*Salvador Mir, TIMA*

17:35 **Computer-Aided-Test Techniques for the Evaluation of AMS DFT**  
*Hervé Naudet, STM*

18:00 **Closing**



**Advance Programme**

**European Nanoelectronics Design Technology Conference**

**Highlights from CATRENE and ENIAC projects**

**DTC**

**June 23 – 24, 2010**

**MINATEC<sup>®</sup>, Grenoble, France**  
**Co-located with MINATEC Crossroads**

**Chair:** Ahmed Jerraya, CEA-LETI, France  
**Co-Chairs:** Mario-Diaz Nava, ST  
Denis Rousset, STEricsson,

**For More Information:**

<http://www.minatec-crossroads.com/dtc>

**For Venue:**

<http://minatec.congres-scientifique.com/crossroads2010/>

